

Response Under 37 C.F.R. §1.116
Expedited Procedure
Examining Group 1765

Section I. (Amendments to the Claims)

Following is a listing of claims 1-22 as amended herein, with markings to show changes made:

1. (Currently amended) A method for fabricating a precision polysilicon resistor comprising:
 - providing a structure that includes at least one polysilicon resistor device region and at least one other type of device region, said at least one polysilicon resistor device region comprising a polysilicon layer;
 - selectively performing an ion implant and an activation anneal in the at least one other type of device region forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor;
 - subsequently, forming a protective dielectric layer overlying said polysilicon layer in said at least one polysilicon resistor device region; and
 - subsequently, providing a predetermined resistance value to said polysilicon layer in said at least one polysilicon resistor device region.
2. (Original) The method of Claim 1 wherein said at least one polysilicon device region comprises a semiconductor substrate, an optional first dielectric located on the substrate, said polysilicon layer located on the substrate or the optional first dielectric and a second dielectric layer located on the polysilicon layer.
3. (Cancelled).
4. (Original) The method of Claim 1 further comprising forming a patterned photoresist atop the at least one polysilicon resistor device region to protect the region during said selective ion implant.
5. (Original) The method of Claim 1 wherein said protective dielectric layer is a nitride.

BEST AVAILABLE COPY

Response Under 37 C.F.R. §1.116
Expedited Procedure
Examining Group 1765

6. (Original) The method of Claim 1 wherein said step of providing a predetermined resistance value to said polysilicon layer comprises ion implantation into the polysilicon layer.
7. (Original) The method of Claim 6 wherein said ion implantation comprises p or n-type dopants.
8. (Original) The method of Claim 7 wherein said ion implantation provides said polysilicon layer with a dopant concentration of from about 1×10^{14} to about 1×10^{21} atom/cm³.
9. (Original) The method of Claim 6 further comprising an annealing step after said ion implantation.
10. (Original) The method of Claim 9 wherein said annealing step is performed in an inert gas ambient that may optionally be mixed with less than about 10% oxygen.
11. (Original) The method of Claim 1 further comprising exposing end portions of said polysilicon layer after said step of providing a predetermined resistance value to said polysilicon layer.
12. (Original) The method of Claim 11 further comprising providing silicide contacts on the exposed polysilicon layer.
13. (Original) The method of Claim 12 wherein said silicide contacts are formed using a silicidation process.
14. (Original) The method of Claim 13 wherein said silicidation process comprises depositing a conductive metal and annealing to cause reaction of the conductive metal with the underlying polysilicon layer thereby forming said silicide contacts.

BEST AVAILABLE COPY

Response Under 37 C.F.R. § 1.116
Expedited Procedure
Examining Group 1765

15. (Original) The method of Claim 14 wherein said conductive metal is selected from the group consisting of Co, Ni, Ti, W and alloys thereof.
16. (Original) The method of Claim 15 wherein said conductive metal is Co or Ti.
17. (Currently amended) A process for fabricating a precision polysilicon resistor comprising:
performing a rapid thermal anneal for an emitter/FET activation process on a wafer or chip having a partially formed polysilicon resistor having a polysilicon layer, said rapid thermal anneal forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor;
subsequently, depositing a protective layer over the polysilicon layer to protect the polysilicon layer against subsequent silicide processing;
subsequently, ion implanting a dopant into the polysilicon layer through the protective layer; and
subsequently, performing silicide processing to form the precision polysilicon resistor.
18. (Original) The method of Claim 17 wherein the step of performing silicide processing includes performing a silicide formation thermal anneal followed by a silicide conversion thermal anneal to activate the resistor polysilicon ion implant dopant.
19. (Original) The method of Claim 17 wherein the step of performing silicide processing includes performing a silicide formation thermal anneal followed by a silicide conversion thermal anneal.
20. (Original) The method of Claim 17 wherein said protective layer comprises a nitride.

BEST AVAILABLE COPY